WBS 6.5.1.1
Tile Main Boards

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U.S. ATLAS HL-LHC Upgrade Director's Review
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Cost Estimation: Materials

- Have excellent basis of cost from demonstrator: $1082/board
  - Based on production of 1100 boards, preproduction of 100
- Cost drivers (we have quotes for everything):
  - Propose to purchase all but passive components in two batches
  - PCB: $240 in quantity 550
  - PCB assembly in quantity 550: $182
    - Labor charge here: need to debug (mostly due to ball grid arrays)
  - IC's and connectors: DC-DC, ADC, FPCAs: $564
    - assuming 20% discount from retail (Arrow Electronics)
  - Passive components: $96 (buy in one batch)
- We know a lower limit on the yield/repair from making 12
  - This of course was early in the learning curve
  - Propose to use same vendors who suffered through demonstrator with us

Cost Estimation: Labor

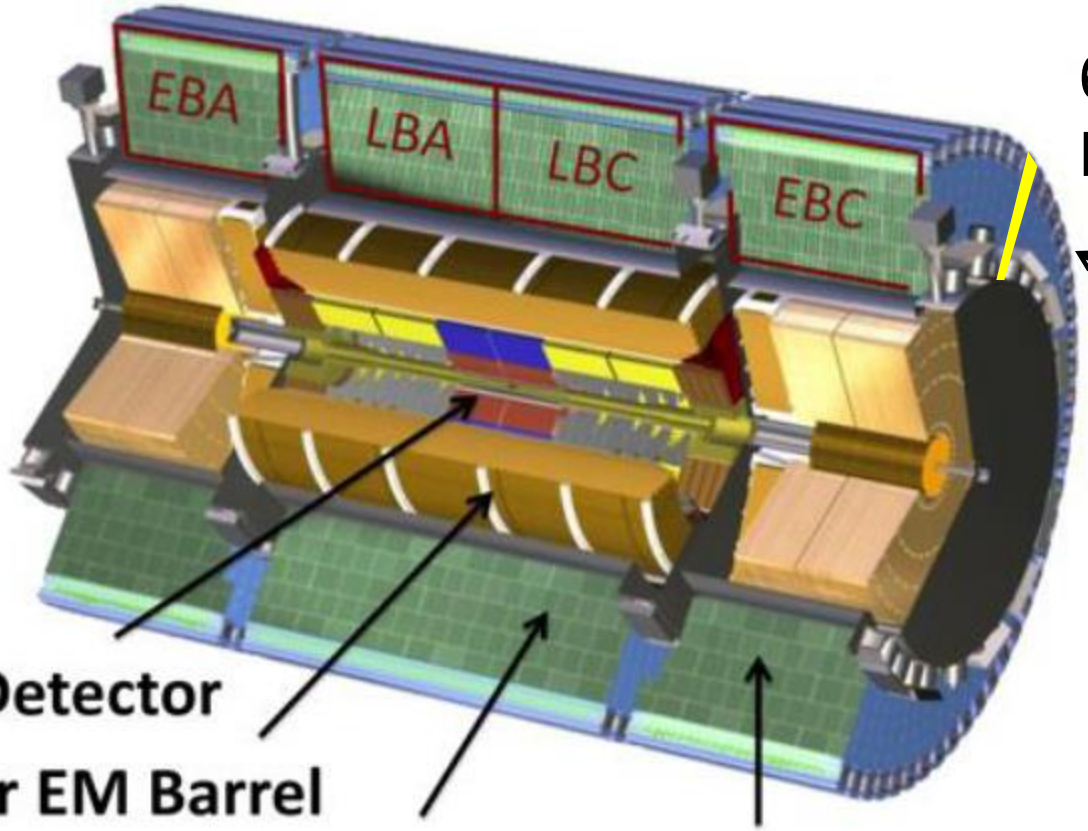
- Very similar task to original Motherboard production
  - So our estimates agree with old cost book
  - Production time driven by burn-in: 5 stations, 4 MB/station, 5 days
    - 1200 MB *5d * 8 hr/d /(5*4 boards) imply 1 year, 1.4 FTE to monitor (students)
    - Apply 50% efficiency factor: 18 months, but distribute over FY21,22
    - Repair: 1200 MB * 10% fail * 6 hr = 0.4 FTE
    - Total production labor: 4.6 FTE
      - 0.6 (EE,ET) for procurement, PCB testing and assy debugging
      - 3.6 FTE (EE,ET,students) for burn-in
      - 0.4 (EE,ET) repair
    - Shipping: 0.15 FTE (ET) … we know well how much time this takes and cost
    - Acceptance, etc, at CERN: 0.4 FTE EE over 4 years
      - Teach and monitor CERN personnel doing test, assembly, integration
  - Grand total: 5.15 FTE = 1.20 EE, 1.95 ET, 2.00 students
  - NB: students cost effective and good; no IDC on e-shop labor (EE,ET)

Cost Estimation: Travel

- Very modest local travel to Schaumberg for PCB assembly: $500
- Travel to CERN and Clermont-Ferrand
  - 2 trips per year for EE in FY21-24
  - Attend expert weeks and general system integration issues
  - Estimate $3.86k/week-long trip including IDC (it's what we pay now)

The Current Tile Calorimeter

4 “barrels”, 256 modules



64 ϕ Wedges
R: 2.28-3.87m

LV “finger” boxes

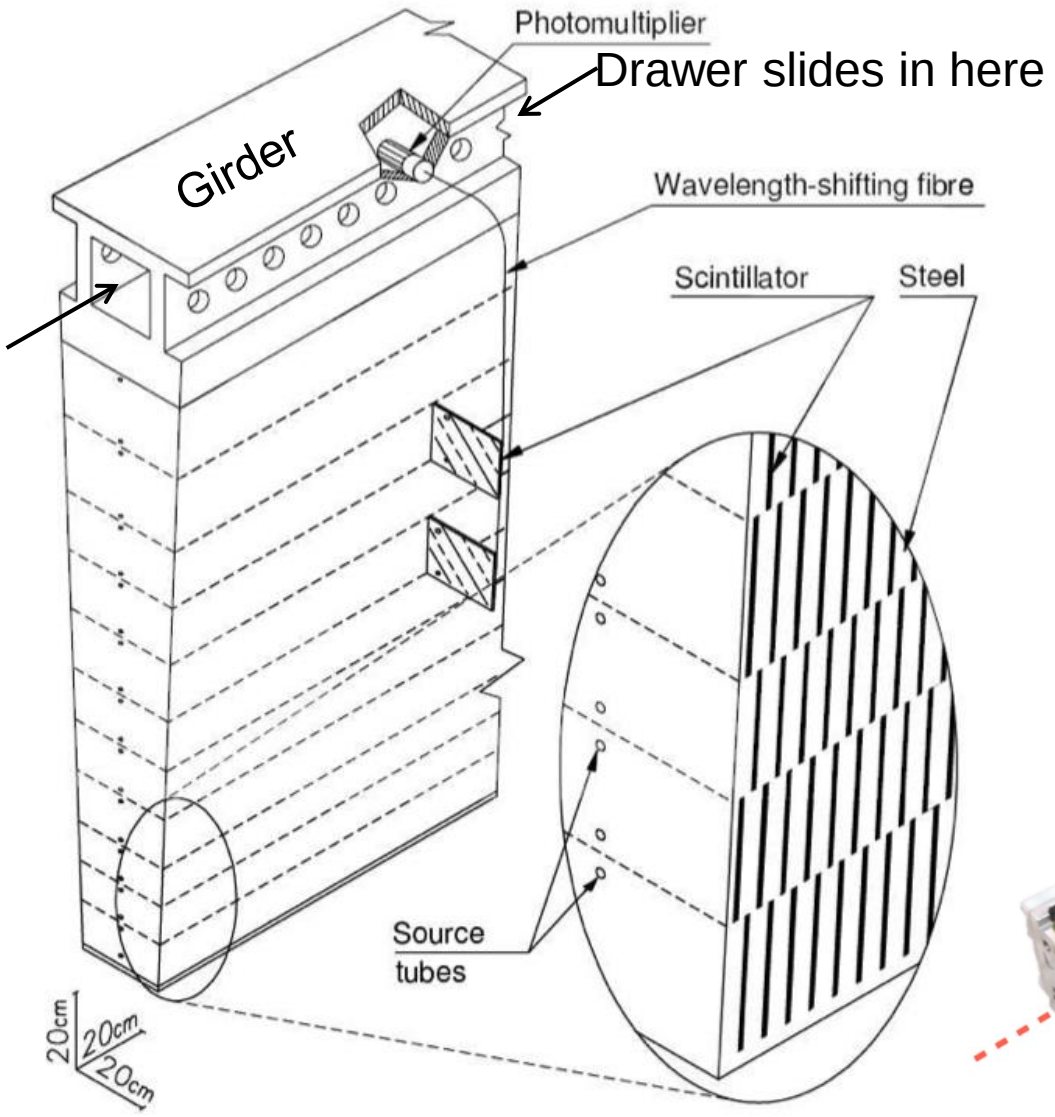
Inner Detector

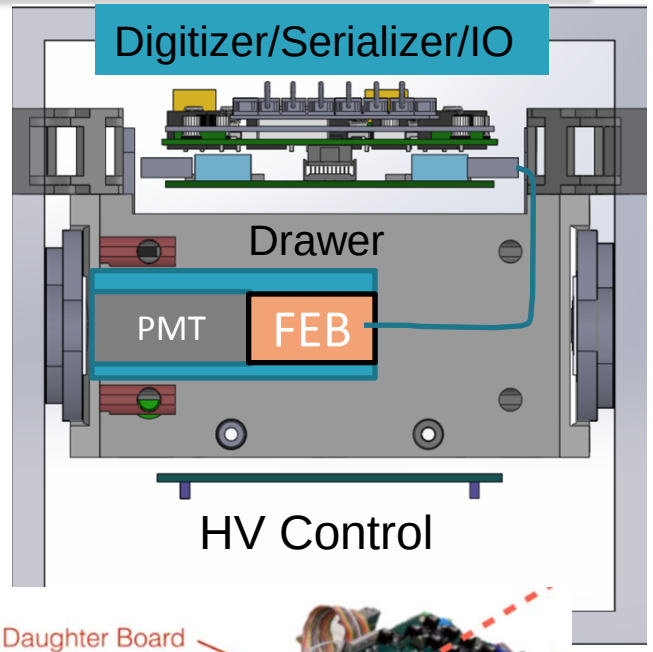
LAr EM Barrel

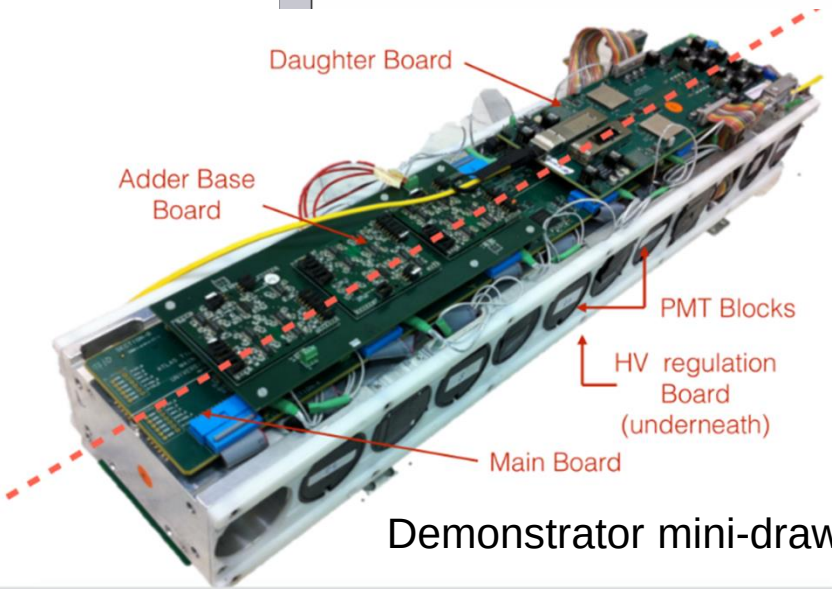
Tile Barrel

Tile Extended Barrel

Tile Wedge Structure

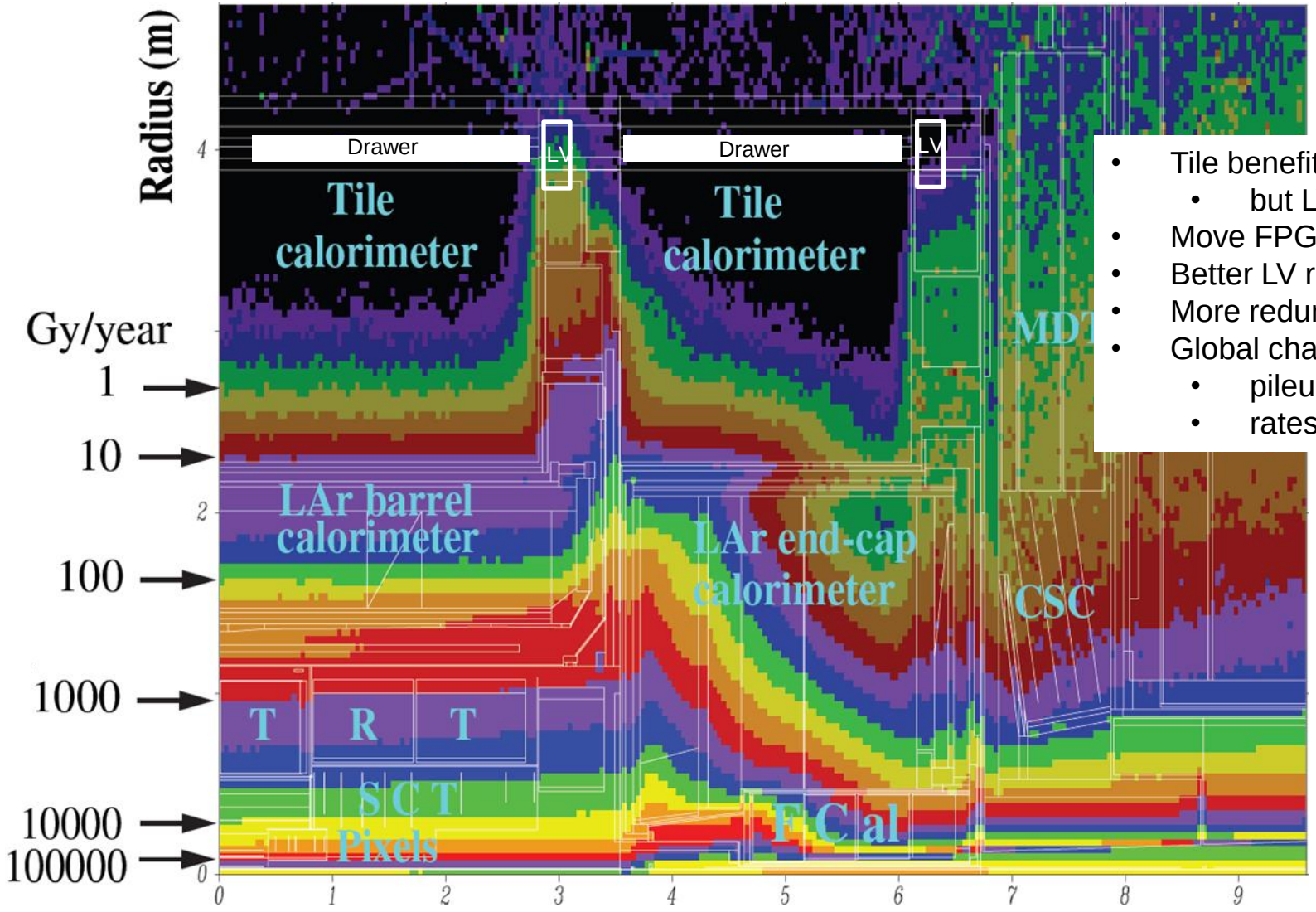






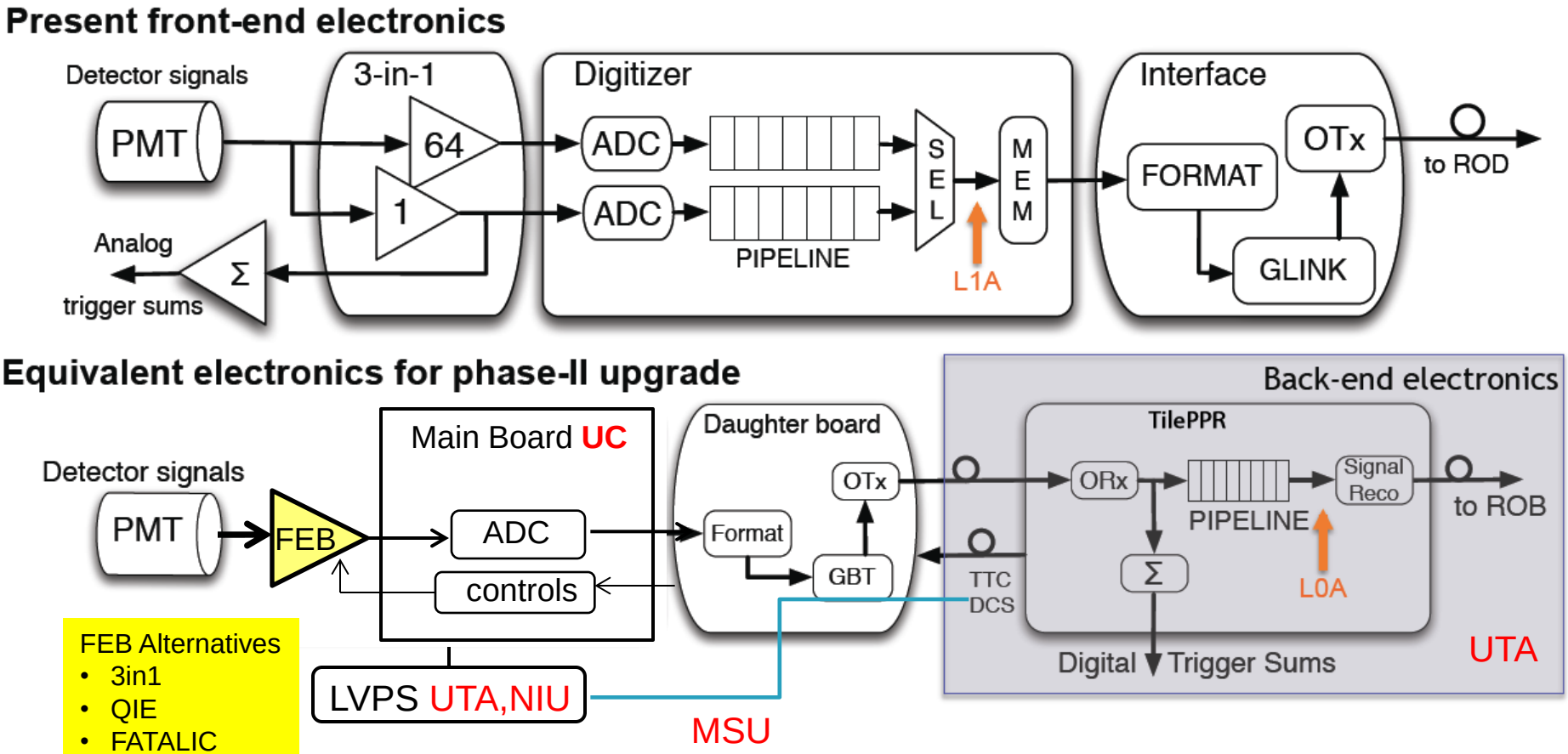
Demonstrator mini-drawer

Old Radiation Map (100 fb^{-1})



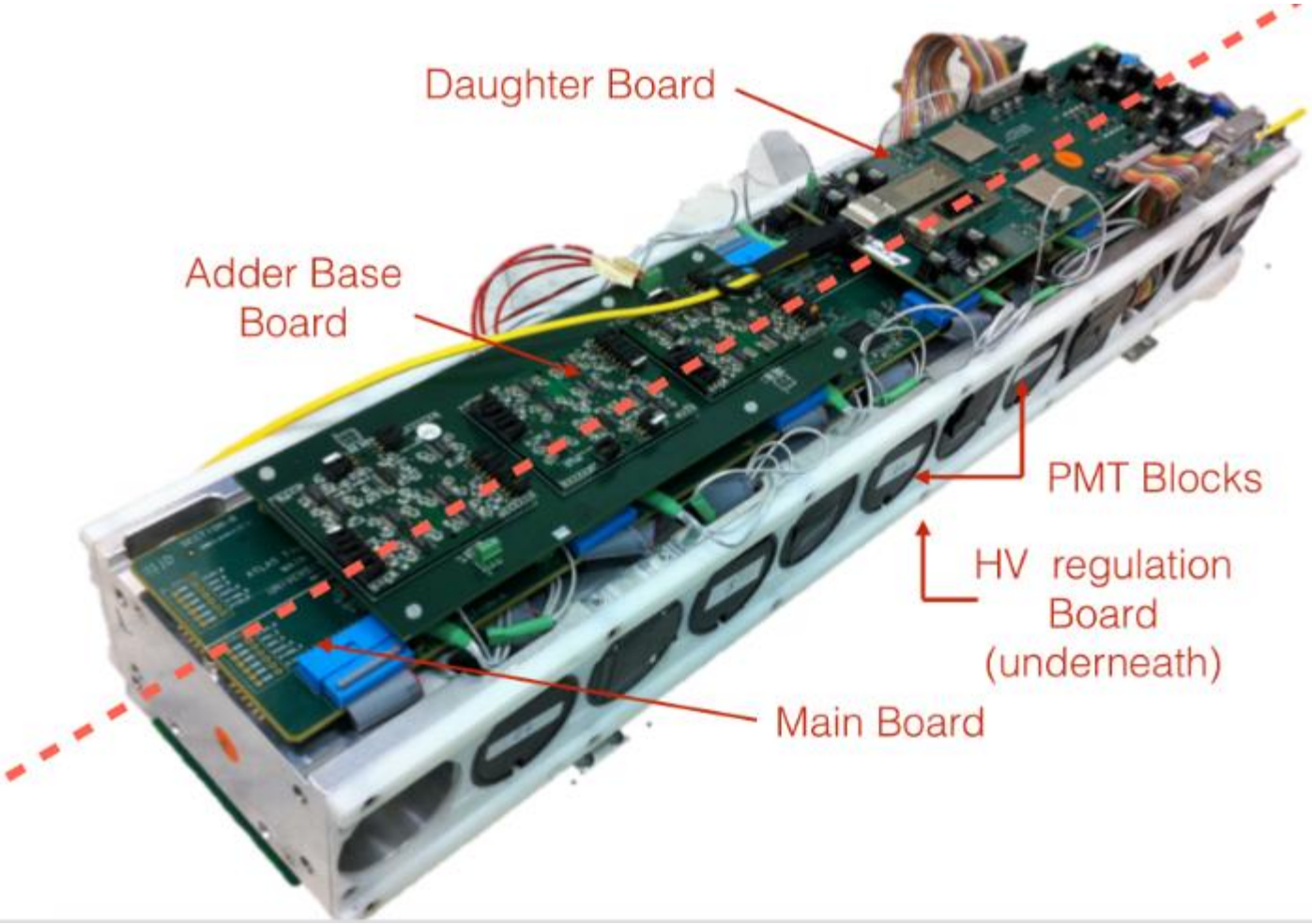
- Tile benefits from shielding
  - but LVPS in n-plume
- Move FPGAs in more
- Better LV rad tolerance
- More redundancy
- Global challenges:
  - pileup: μ=140-200
  - rates, latency

New vs Old Electronics



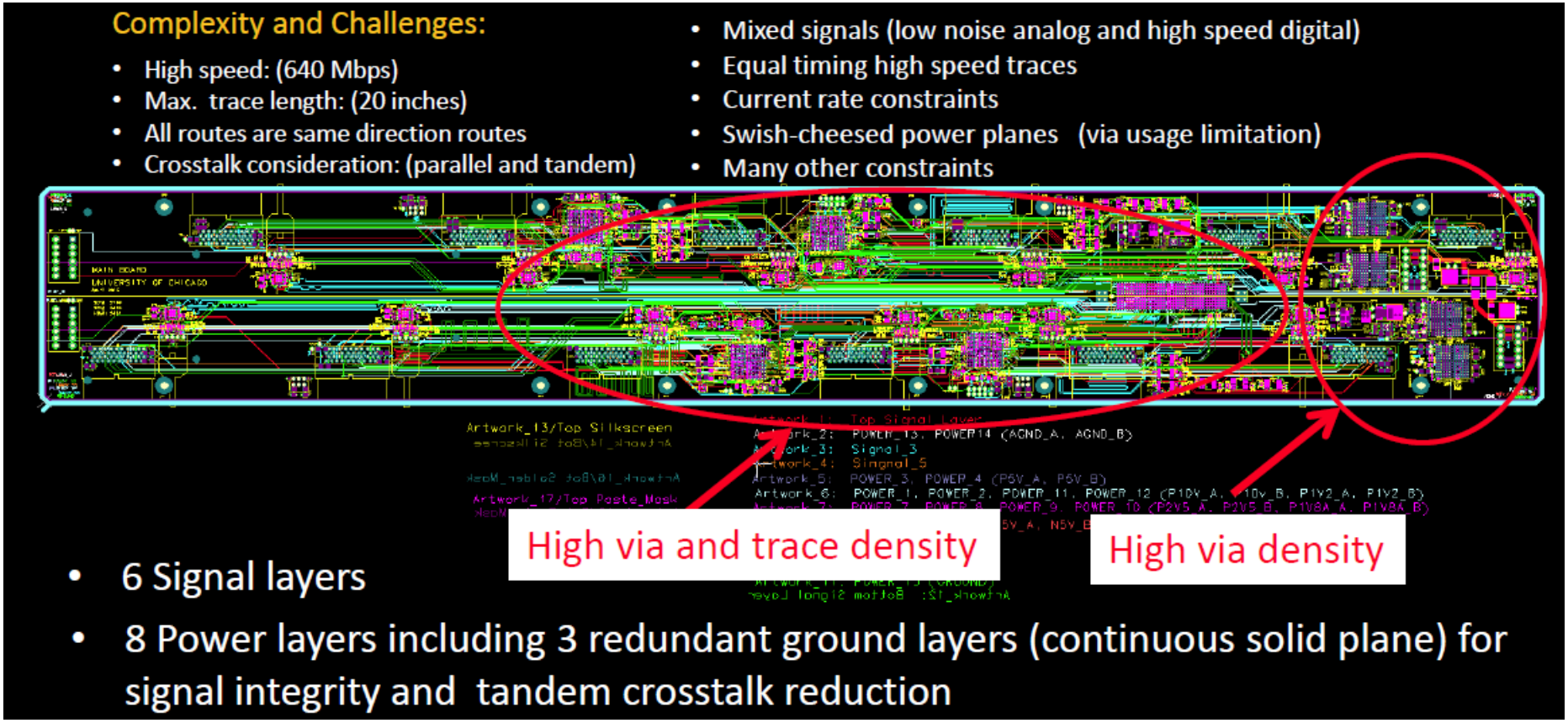
NB: New electronics already prototyped (“Demonstrator”)

A Demonstrator Mini-drawer



6.5.1.1: Main Board (UC)

- interface between FE amplifier/shaper and fast communications DaughterBoard
- 69 cm length , 16 layer board; 1024 needed
- Supplies LV levels, controls, digitization
- into 3rd prototype version for demonstrator



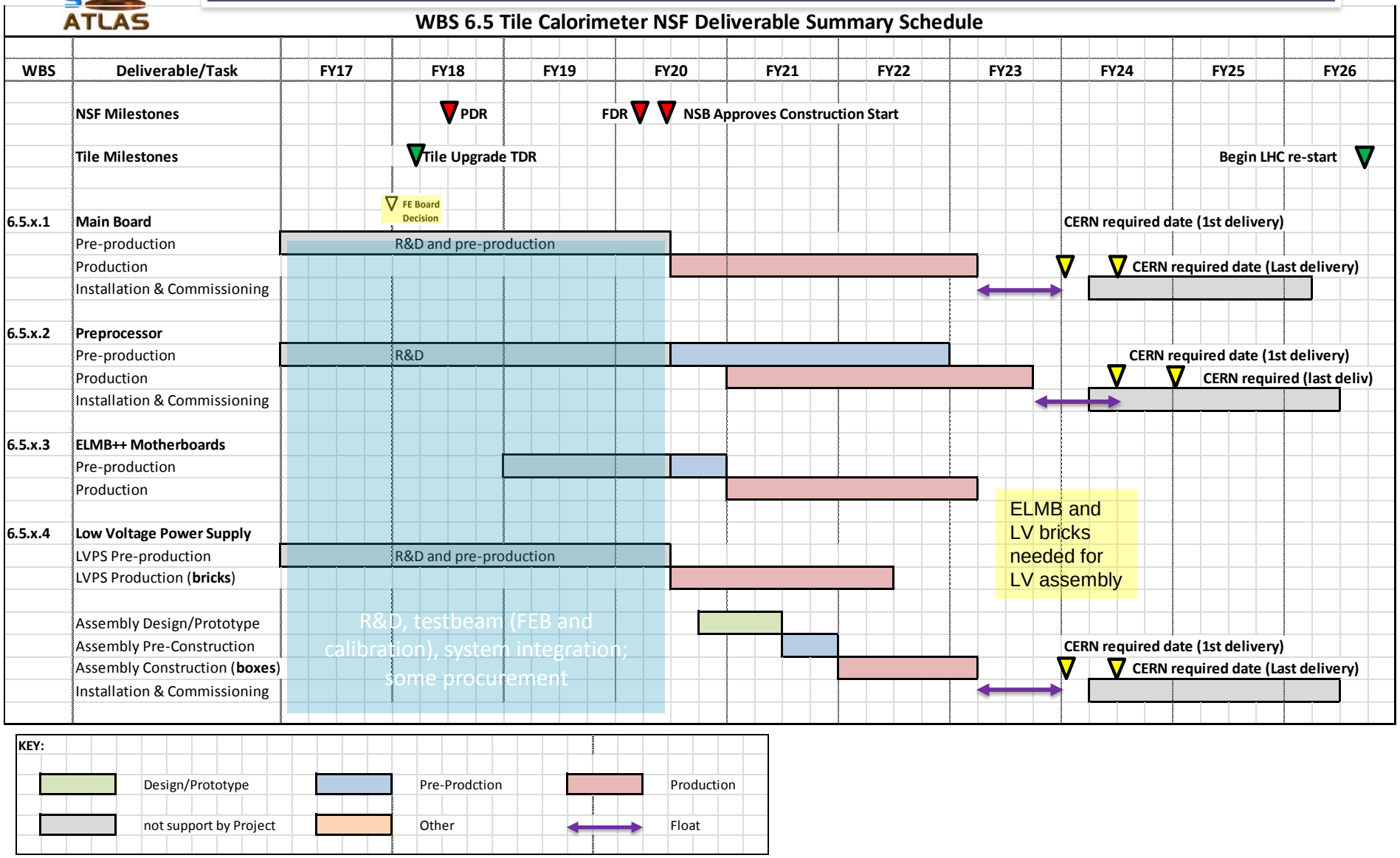
Research and Development

The Demonstrator Program

- R&D from USATLAS to build and evaluate demonstrators
  - 3in1, QIE front-end cards and Main Boards produced for demonstrator
  - LV, HV control boards designed and prototyped; LVboxes produced
  - Radiation certification of components and development of rad-hard optical modulator
- Good progress so far:
  - 2015: beam test of 3in1-based demonstrator (successful!)
  - 2016: two more beam tests to evaluate ASIC FEB's
  - 2016: simulations; which FEB handles pileup best?
  - 2017: experience with a demonstrator in ATLAS detector
  - 2017-2020: final integrated design, prototype, testing
    - Includes test beam running to measure Jet Energy Scale and radiation certification
- NSF MREFC funding start is FY20 Q3 $\Rightarrow$ "R&D" includes some pre-production

Level 4 Timeline

Driven by CERN Scoping Document and installation schedule



Cost and Effort Estimates

(more details in the BOEs)

- The cost estimates are rather detailed and based on:
  - actual or similar Bill of Materials with quotes from vendors
    - assuming 20% discount from retail (our experience is more like 30-40%)
  - effort estimates based on the original construction, refined by the recent experience building and testing boards for the demonstrator
    - The FEB, Main Boards, LVPS bricks and boxes are very similar in production scope to the current versions … which we built!
    - The PreProcessor cards are new, ATCA technology, but we have the experience of constructing the demonstrator prototypes

Risks

- Risks all low because of working demonstrator prototype
- Cost risk: very low
  - have BOMs from demonstrator; cost goes down for CERN bulk purchases
  - only assuming 20% bulk discount from retail (it's usually higher)
  - FPGAs likely to go down in cost, but we are using quotes for FY18
- Schedule risk: low
  - not negligible, because Tile installation is early in the schedule
  - but significant float in proposed schedule (12-19 months)
  - main risk: delivery of FEB, LV bricks from non-US institutes
- Technical risk: very low
  - Tile is in lower radiation area
  - electronics design not too sophisticated; often similar to current design
  - main risk: replacement component does not meet radiation standard

Front-end Alternatives

- Chicago's 3in1 FEB and associated Main Board are the **default**
  - Performing well in tests and radiation certification
  - Most complicated MB (has ADCs); total MB cost ≈ total FEB cost
  - Shapes pulse and has dual gain ranges
- Two ASIC alternatives being evaluated
  - QIE (ANL): boxcar integrator, 5 gain ranges
  - FATALIC (LPC Clermont-Ferrand): shaped pulse, 3 gain ranges
  - Downselect: by end of CY 2017
- Whatever alternative is chosen, UChicago and LPC will share:
  - Chicago makes the Main Boards (simpler for the ASIC alternatives)
  - LPC manufactures the front-end cards
    - This makes sense especially if an ASIC is used (single point of contact)